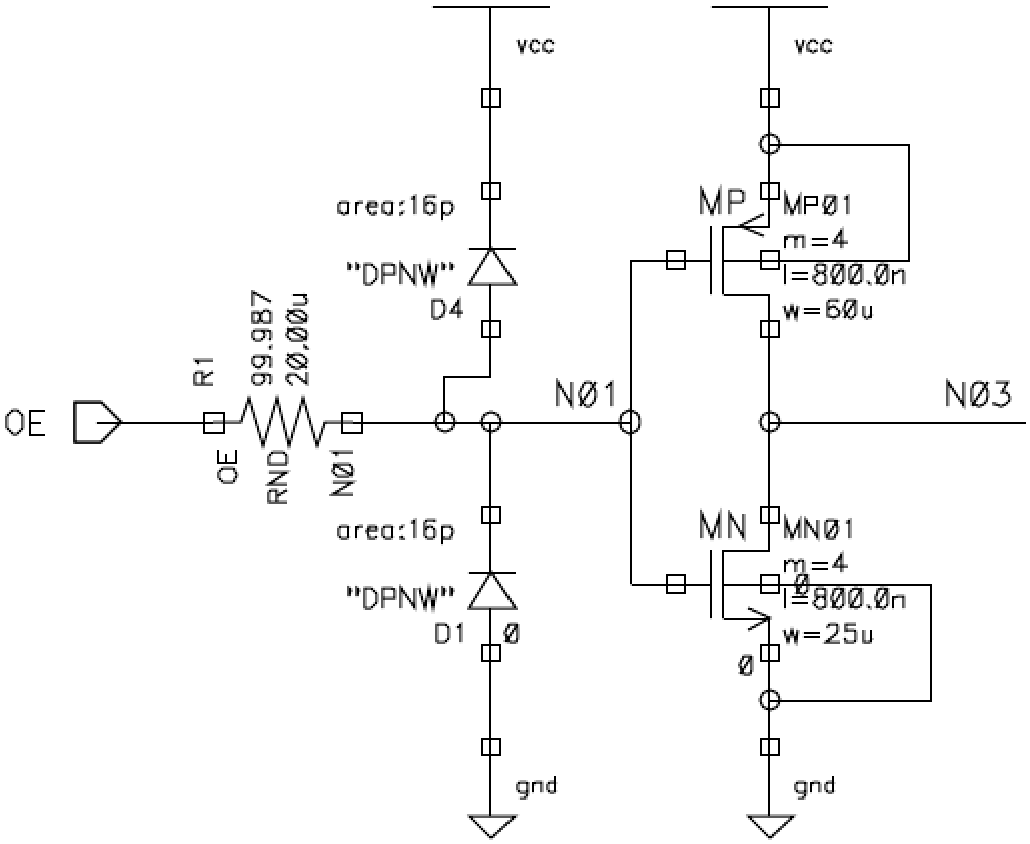
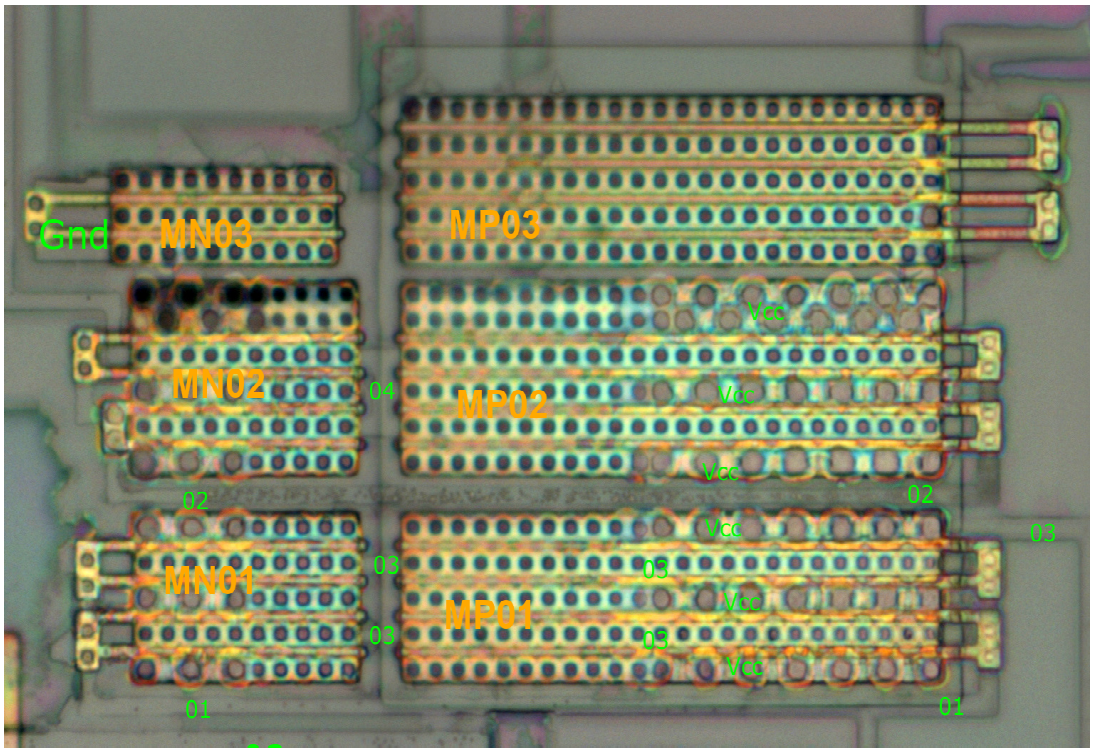
LVC1G126 Extraction Notes.

1. The unit input transistor size is not as small as one might guess.

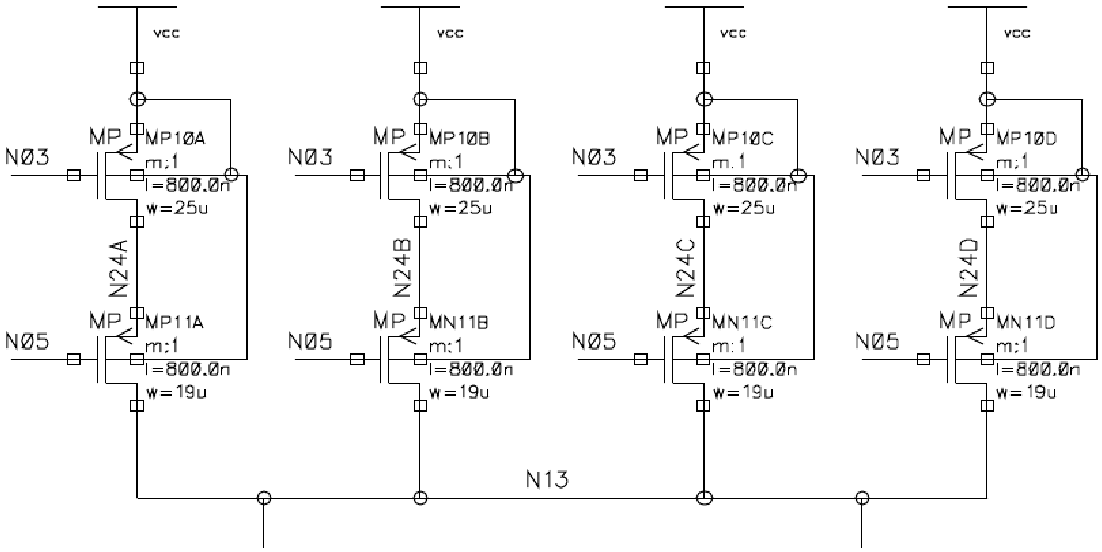
The PMOS is 4 fingers 60 microns in width while the NMOS is 4 sections 25 microns in width. The actual Poly Gate Length seems to be drawn at about 0.9 microns.



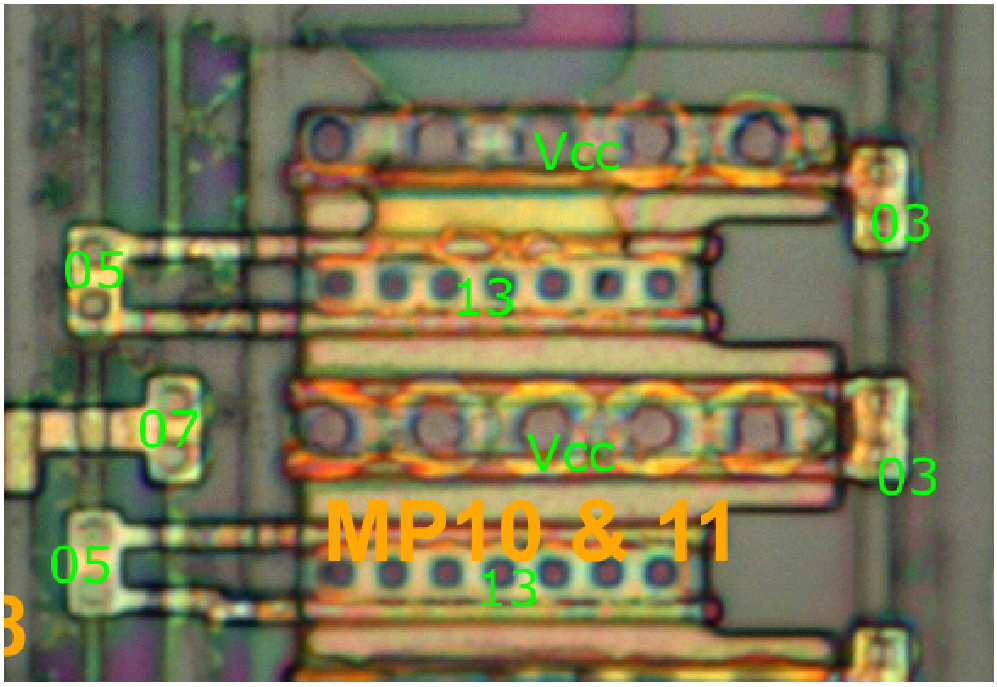
2. The inverters are drawn with NMOS and PMOS ends abutted to save on layout space. The gate poly is stretched for routing. Poly view followed by metal 1 view. Node 3 and Node 4 pass through respective inverters.

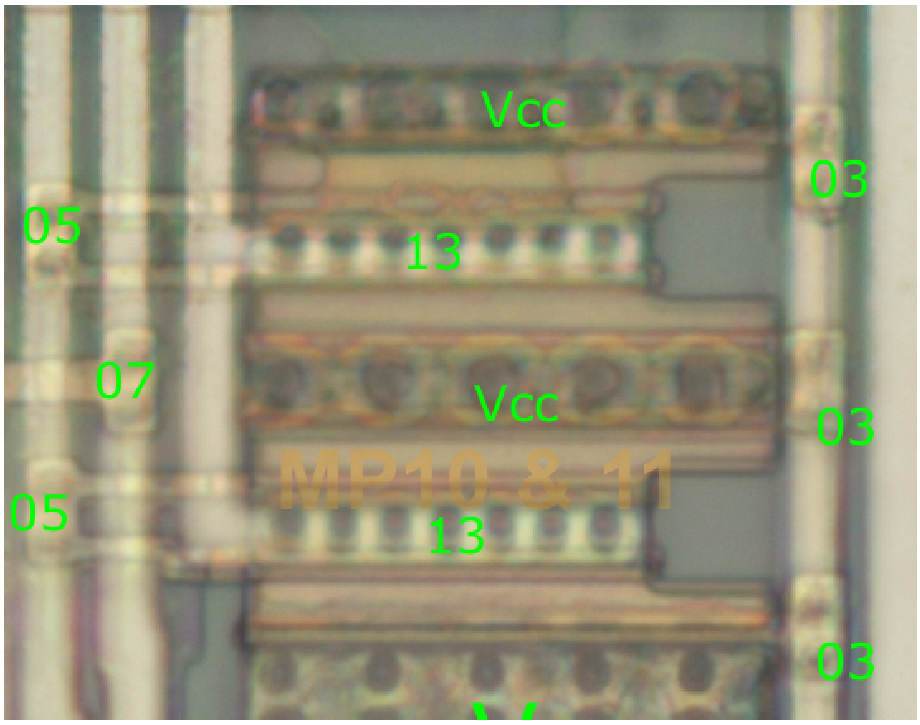


3. Compound Transistors can be drawn as a way to implement logic functions. In this case it was decided that the width of the MP10 portion be 25u while the width of the MP11 portion be 19u. Nodes N24A, N24B, N24C, and N24D are floating nodes with no contacts or metal connections.



3.(continued) Also note the Gate Poly is stretched to allow for routing.
Poly view followed by Metal 1 view.



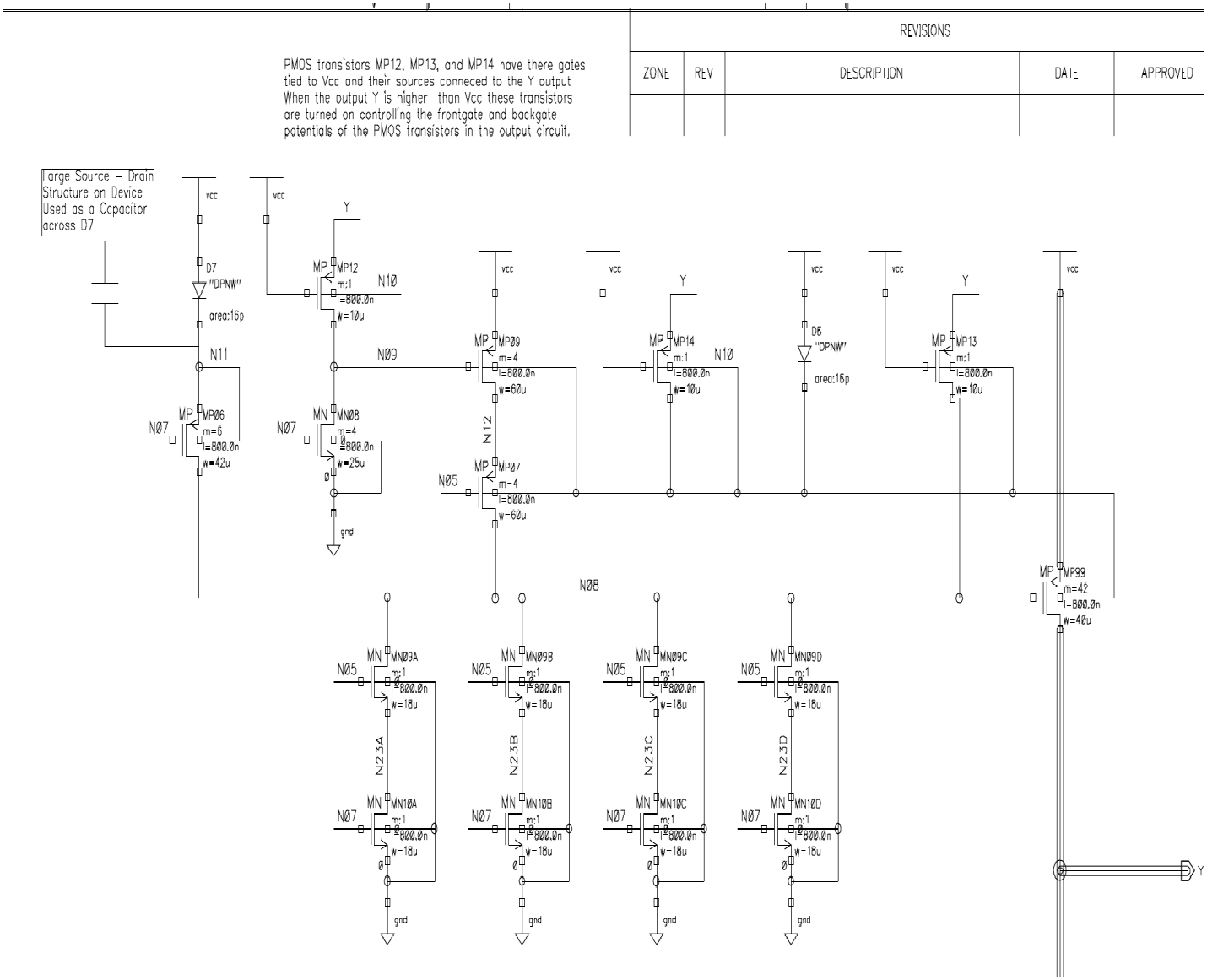


3.The Ioff circuitry. A key feature of the LVC family is to allow a high voltage to be applied to the output while Vcc=0V and have only a very small leakage current to flow.

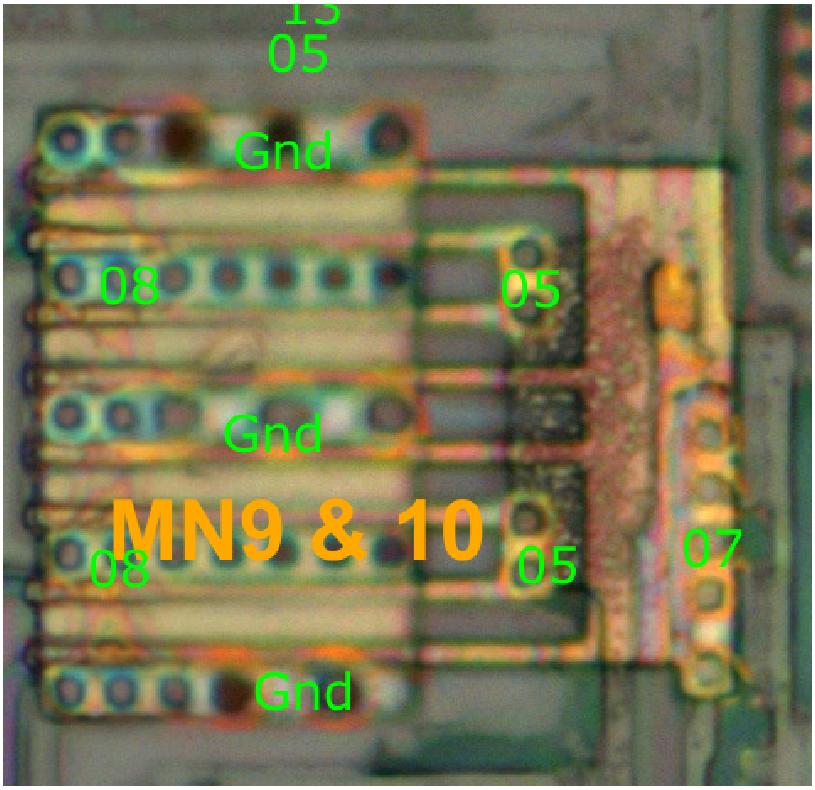
When Vcc=0 and the Y output = 5V
MP13 is turned on and connects node 8, the gate of large PMOS MP99 to output Y..

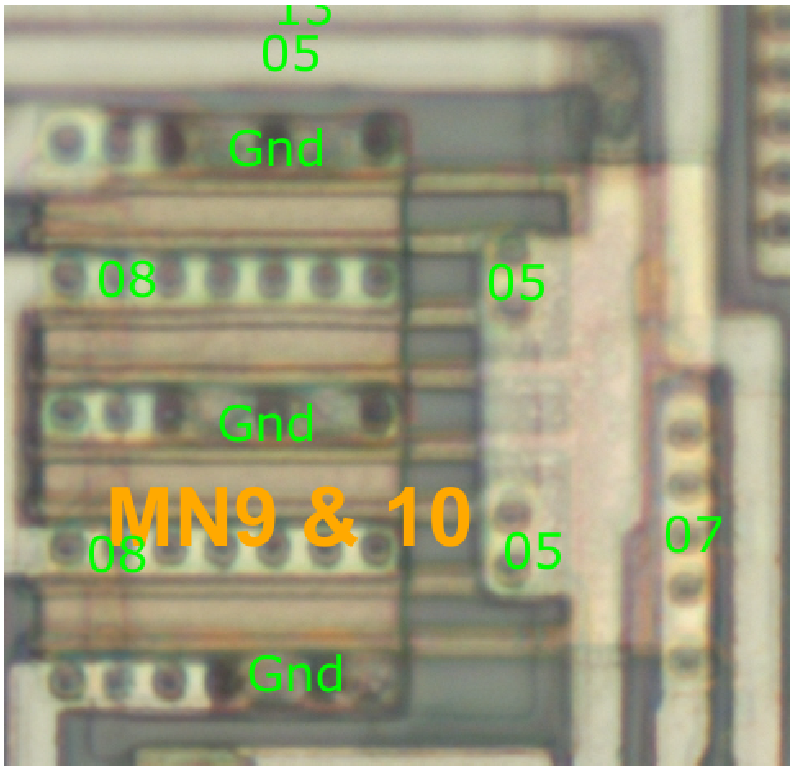
also when Vcc=0 and the Y output = 5V
MP14 is turned on and connects the output Y to node10 the body of MP99. (node10 is also the Body connection for several other of the PMOS transistors).

lastly when Vcc=0 and the Y output =5V
MP12 turns on connecting Y to Node N09 the gate of MP09. This isolates MP07 from Vcc and ends the path of output Y being propagated into the part.



4.The merged transistors MN9 and MN10 are denoted below. This discharges the gate and turns on the large PMOS output. Node 8 is connected to Y during the Ioff Condition





5. Output NMOS

A poly level photo of the edge of the output NMOS reveals that the part is drain extended with the source measuring 2.7 microns and the drain measuring 5.4 microns . The poly appears to be .85microns wide and is not optically different than the poly width on any of the other transistors. The contacts on the Ground fingers are gouged out by the acid that came down the vias between Metal 2 and Metal one during deprocessing.

The output NMOS uses both drain extension and ballast resistors as protection measures.