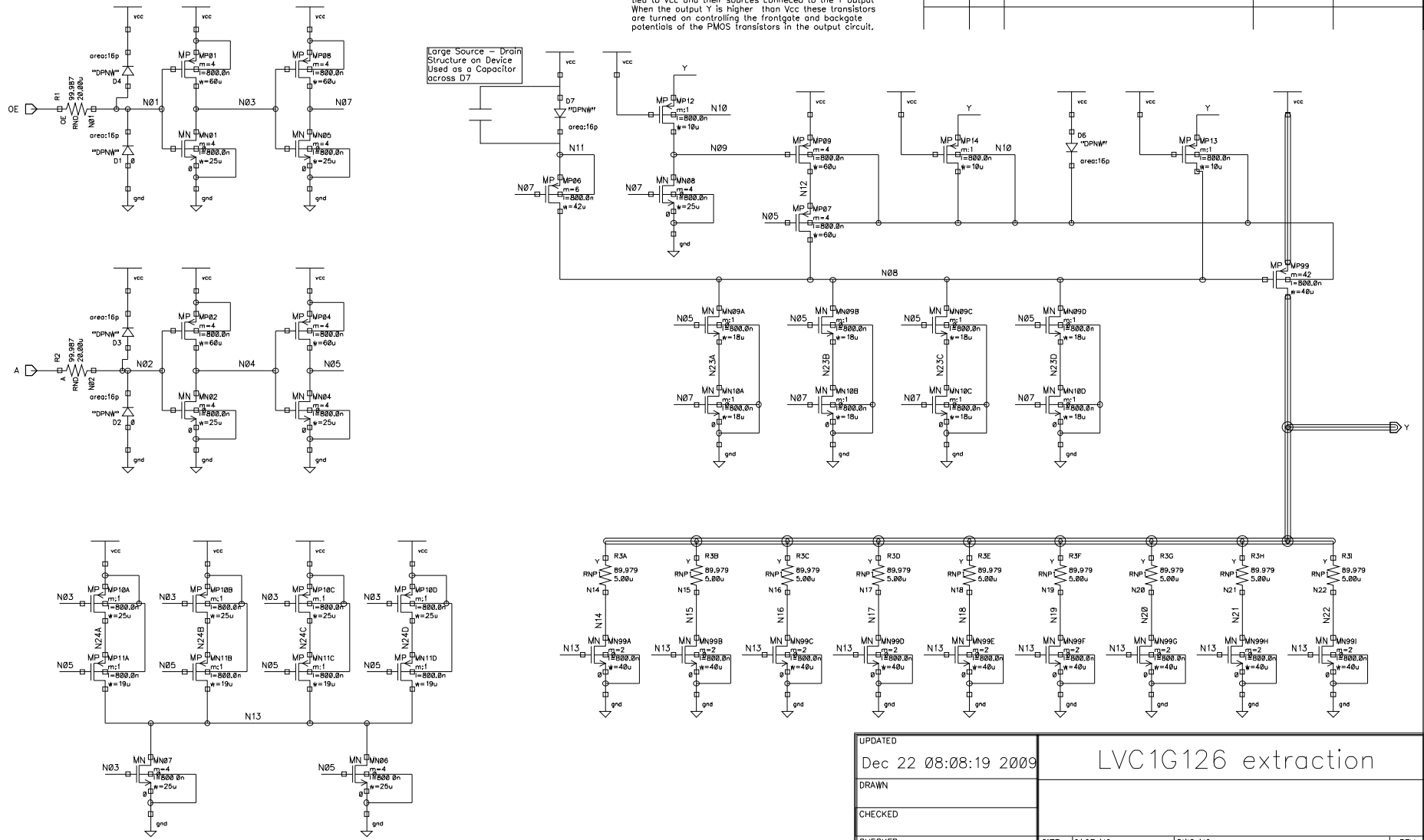
CAGE NO.	DWG NO.	SH	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

PMOS transistors MP12, MP13, and MP14 have there gates tied to Vcc and their sources conneced to the Y output When the output Y is higher than Vcc these transistors are turned on controlling the frontgate and backgate potentials of the PMOS transistors in the output circuit.

Large Source – Drain Structure on Device Used as a Capacitor across D7



UPDATED	LVC1G126 extraction		
Dec 22 08:08:19 2009			
DRAWN			
CHECKED			
CHECKED	SIZE B	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET OF